HT93LC76/LC86

CMOS 8K/16K-Bit Serial EEPROM

Features

- Wide range operating voltage
  - Write: 2.4~5.5V
  - Read: 2.0~5.5V
- Low power consumption
  - Operating: Max. 5mA
  - Standby: Max. 2μA
- User selectable internal organization
  - 8K(HT93LC76): 1024×8 or 512×16
  - 16K(HT93LC86): 2048×8 or 1024×16
- Write operation with built-in timer
- Automatic erase-before-write operation
- Word/chip erase and write operation
- Auto-increment read operation
- Programming Status Indicator
- Software and hardware controlled write protection
- 10-year data retention after 100K rewrite cycles
- 10^6 rewrite cycles per word
- Operating temperature range: –40°C~+85°C
- 8-pin DIP/SOP package

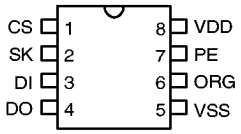
General Description

The HT93LC76/86 is an 8K/16K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 8192/16384 bits of memory are organized into 512/1024 words and each word is 16 bits, when the ORG pin is floating or connected to VDD, or 1024/2048 words and each word is 8 bits, when ORG pin is connected to GND.

These devices also have a Program Enable (PE) pin to allow the user to write protect the entire contents of the memory array.

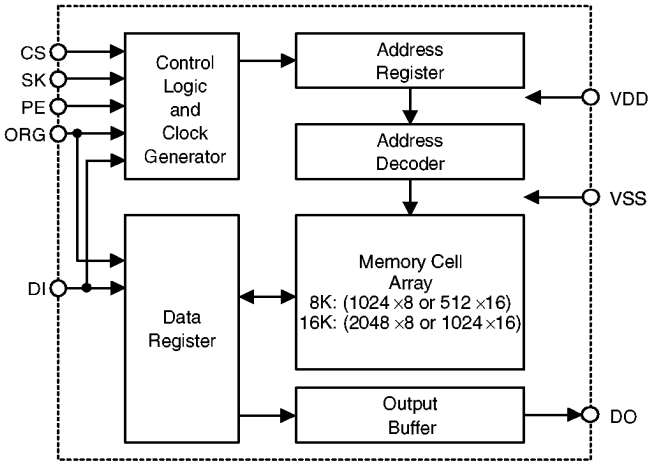
By popular microcontroller, the versatile serial interface including chip select (CS), serial clock (SK), data input (DI) and data output (DO) can be easily controlled.

Pin Assignment



HT93LC76/86
– 8 DIP/SOP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
1	CS	I	Chip select input
2	SK	I	Serial clock input
3	DI	I	Serial data input
4	DO	O	Serial data output
5	VSS	I	Negative power supply
6	ORG	I	Per word 8/16 bits option
7	PE	I	Program enable
8	VDD	I	Positive power supply

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought to LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (T_{CDS}) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (SK)

The serial clock (SK) is used to synchronize the communication between a master device and the 93LC76/86. Opcode, address, and data bits are clocked in on the positive edge of SK. Data bits are also clocked out on the positive edge of SK.

SK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continuous anytime with respect to clock HIGH time (T_{SKH}) and clock LOW time (T_{SKL}). This gives the controlling master freedom in preparing opcode, address, and data. SK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e. waiting for START condition).

SK cycles are not required during the self-timed WRITE (i.e. auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of SK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). SK and DI then become don't care input waiting for a new start condition to be detected.

Data In (DI)

Data in (DI) is used to clock in START bits, opcode, address, and data synchronously with the SK input.

Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the SK input (T_{PD} after the positive edge of SK).

This pin also provides READY/BUSY status information during ERASE and WRITE cycles. READY/BUSY status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip deselect time (T_{CDS}) and an ERASE or WRITE operation has been initiated.

Organization (ORG)

When ORG is connected to VDD or ORG is floated, the (×16) memory organization is selected. When ORG is tied to VSS, the (×8) memory organization is selected. There is an internal pull-up resistor on the ORG pin.

Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is floated or tied to VDD, the device can be programmed. If the pin is tied to VSS, programming will be inhibited. These is an internal pull-up resistor on the PE pin.

Absolute Maximum Ratings*

Supply Voltage .....–0.3V to 6.0V
Input Voltage.....V_{SS}–0.3 to V_{DD}+0.3
Storage Temperature.....–50°C to 125°C
Operating Temperature.....–40°C to 85°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(Ta=–40°C to 85°C)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
		V_{DD}	Conditions			
V_{DD}	Operating Voltage	—	Read	2	5.5	V
		—	Write	2.4	5.5	V
I_{DD1}	Operating Current (TTL Input Level)	5V	DO unload, SK=1MHz	—	5	mA
I_{DD2}	Operating Current (CMOS Input Level)	5V	DO unload, SK=1MHz	—	5	mA
		2~5.5V	DO unload, SK=250kHz	—	5	mA
I_{STB}	Standby Current	5V	CS=SK=DI=0V	—	2	μA
I_{LI}	Input Leakage Current	5V	$V_{IN}=V_{DD}$~V_{SS}	0	1	μA
I_{LO}	Output Leakage Current	5V	$V_{OUT}=V_{DD}$~V_{SS}, CS=0V	0	1	μA
V_{IL}	Low Level Input Voltage	5V	—	0	0.8	V
		2~5.5V	—	0	$0.1V_{DD}$	V
V_{IH}	High Level Input Voltage	5V	—	2	V_{DD}	V
		2~5.5V	—	$0.9V_{DD}$	V_{DD}	V
V_{OL}	Low Level Output Voltage	5V	I_{OL}=2.1mA	—	0.4	V
		2~5.5V	I_{OL}=10μA	—	0.2	V
V_{OH}	High Level Output Voltage	5V	I_{OH}=–400μA	2.4	—	V
		2~5.5V	I_{OH}=–10μA	V_{DD}–0.2	—	V
T_{RW}	Rewriting Times	5V	25°C VDD=5V Block mode (Note 2)	10^6	—	Times/ word
C_{IN}	Input Capacitance (see Note 1)	—	f=250kHz	—	5	pF
C_{OUT}	Output Capacitance (see Note 1)	—	f=250kHz	—	5	pF

Note1: These parameters are periodically sampled but not 100% tested
Note2: The block mode exercises all the cells of the array simultaneously

A.C. Characteristics

(Ta=–40°C to 85°C)

Symbol	Parameter	VDD=5V±10%		VDD=3V±10%		VDD=2V*		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	0	2000	0	500	0	250	kHz
t_{SKH}	SK High Time	250	—	1000	—	2000	—	ns
t_{SKL}	SK Low Time	250	—	1000	—	2000	—	ns
t_{CSS}	CS Setup Time	50	—	200	—	200	—	ns
t_{CSH}	CS Hold Time	0	—	0	—	0	—	ns
t_{CDS}	CS Deselect Time	250	—	1000	—	1000	—	ns
t_{DIS}	DI Setup Time	100	—	400	—	400	—	ns
t_{DIH}	DI Hold Time	100	—	400	—	400	—	ns
t_{PD1}	DO Delay to '1'	—	500	—	2000	—	2000	ns
t_{PD0}	DO Delay to '0'	—	500	—	2000	—	2000	ns
t_{SV}	Status Valid Time	—	500	—	2000	—	—	ns
t_{HZ}	DO Disable Time	—	100	—	400	—	400	ns
t_{PR}	Write Cycle Time	—	5	—	5	—	—	ms

*For Read Operating Conditions Only

A.C. Test Conditions

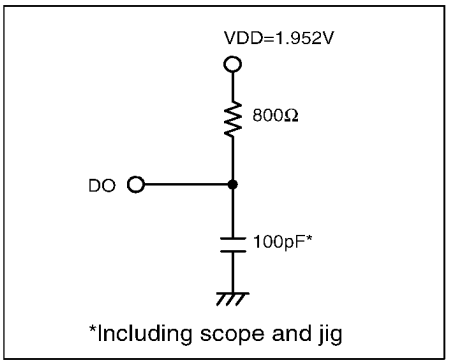
Input pulse levels: 0V to 3V

Input rise and fall time: 5ns (1V to 2V)

Input and output timing reference levels: 1.5V

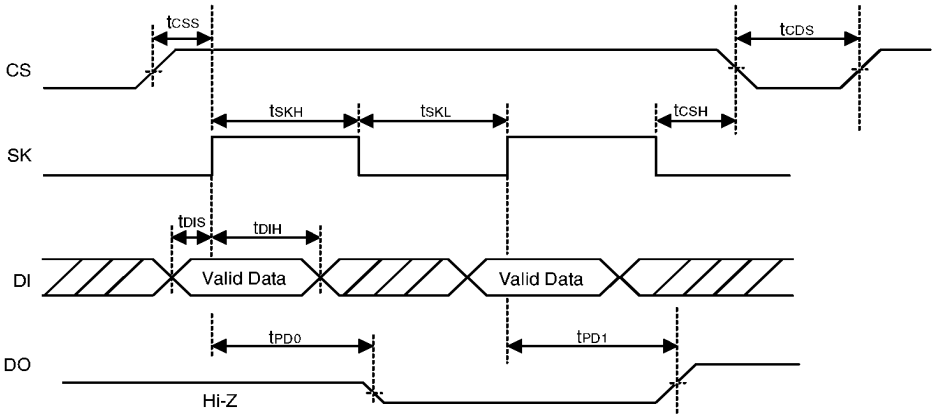
Frequency: 1MHz

Output load: See Figure right



Output Load Circuit

Timing Diagrams



Functional Description

The HT93LC76/86 is accessed via a three-wire serial communication interface. The device is arranged into 512/1024 words by 16 bits or 1024/2048 words by 8 bits depending on the ORG pin whether it is connected to VDD (or floating) or GND. The HT93LC76/86 contains 7 instructions: READ, ERASE, WRITE, EWEN, EWDS, ERAL and WRAL. When the user selectable internal organization is arranged into 512/1024×16 (1024/2048×8), these instructions are all made up of 13(14) bits data: 1 start bit, 2 op code bits and 10(11) address bits.

By using the control signal CS, SK and data input signal DI, these instructions can be given to the HT93LC76/86 separately. These serial instruction data presented at the DI input will be written into the device at the rising edge of SK. During the READ cycle, DO pin acts as the data output and during the WRITE or ERASE cycle, DO pin indicates the BUSY/READY status. When the DO pin has to be active for read data or as a BUSY/READY indicator the CS pin must be high; otherwise DO pin will be in a high-impedance state. For successful instructions, CS must be low once after the instruction is sent. After the power is on, the device is default in the EWDS state. And, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. Following are the functional descriptions and timing diagrams of all 7 instructions.

READ

The READ instruction will stream out data at a specified address on the DO pin. The data on DO pin changes during the low-to-high edge of SK signal. The 8 bits or 16 bits data stream is preceded by a logical '0' dummy bit. Irrespective of the condition of the EWEN or EWDS instruction, the READ command is always valid and independent of these two instructions. After the data word has been read the internal address will be automatically incremented by 1 allowing the next consecutive data word to be read out without entering further address data. The address will wrap around with CS High until CS returns to LOW.

EWEN/EWDS

The EWEN/EWDS instruction will enable or disable the programming capabilities. At both the power-on and power-off state the device is automatically entered the disable mode. Before a WRITE, ERASE, WRAL or ERAL instruction is given, the programming enable instruction EWEN must be issued, otherwise the ERASE/WRITE instruction is invalid. After the EWEN instruction is issued, the programming enable condition remains until power is turned off or a EWDS instruction is given. No data can be written into the device in the programming disabled state. By so doing, the internal memory data can be protected.

ERASE

The ERASE instruction erases data at the specified addresses in the programming enable mode. After the ERASE op-code and the specified address have been issued, the data erasing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for internal erasing, so the SK clock is not required. During internal erasing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instructions can be executed.

WRITE

The WRITE instruction writes data into the device at the specified addresses in the programming enable mode. After the WRITE op-code and the specified address and data have been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for internal writing, so the SK clock is not required. The auto-timing write cycle includes an automatic erase-before-write capability. So, it is not necessary to erase data before the WRITE instruction. During the internal writing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instructions can be executed.

ERAL

The ERAL instruction erases the entire 512/1024×16 or 1024/2048×8 memory cells to logical '1' state in the programming enable mode. After the erase-all instruction set has been issued, the data erasing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the erase-all operation, so the SK clock is not required. During the internal erase-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed. The ERAL instruction is guaranteed at V_{DD}=5V±10%.

WRAL

The WRAL instruction writes data into the entire 512/1024×16 or 1024/2048×8 memory cells in the programming enable mode. After the write-all instruction set has been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the write-all operation, so the SK clock is not required. During the internal write-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed. The WRAL instruction is guaranteed at V_{DD}=5V±10%.

Instruction Set for HT93LC76

Instruction	Comments	Start bit	Op Code	Address ORG=0 ×8	Address ORG=1 ×16	Data ORG=0 ×8	Data ORG=1 ×16
READ	Read data	1	10	XA9~A0	XA8~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	XA9~A0	XA8~A0	—	
WRITE	Write data	1	01	XA9~A0	XA8~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXXXX	11XXXXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXXXX	00XXXXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXXXX	10XXXXXXXX	—	
WRAL	Write All	1	00	01XXXXXXXXX	01XXXXXXXX	D7~D0	D15~D0

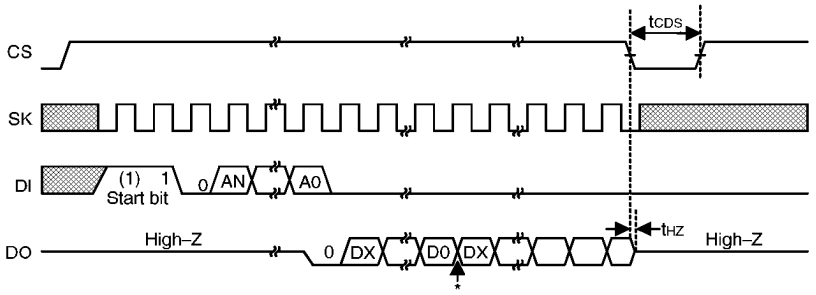
Instruction Set for HT93LC86

Instruction	Comments	Start bit	Op Code	Address ORG=0 ×8	Address ORG=1 ×16	Data ORG=0 ×8	Data ORG=1 ×16
READ	Read data	1	10	A10~A0	A9~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	A10~A0	A9~A0	—	
WRITE	Write data	1	01	A10~A0	A9~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXXXX	11XXXXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXXXX	00XXXXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXXXX	10XXXXXXXX	—	
WRAL	Write All	1	00	01XXXXXXXXX	01XXXXXXXX	D7~D0	D15~D0

Note: X stands for "don't care"

Instruction Timing

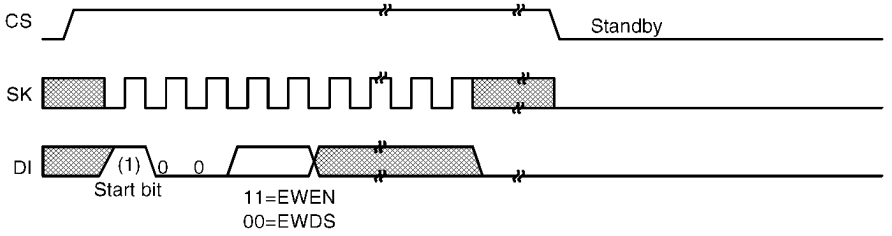
READ



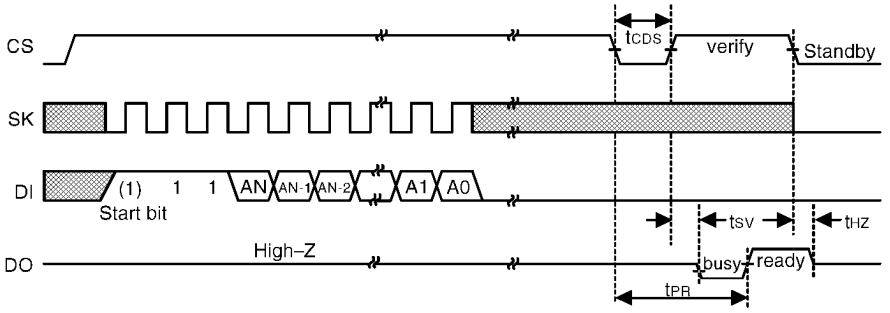
* Address bit A9 becomes a “don't care” (×16 mode) on 93LC76
* Address bit A10 becomes a “don't care” (×8 mode) on 93LC76
* Address pointer automatically cycles to the next word

Mode	(×16)	(×8)
AN	A9	A10
DX	D15	D7

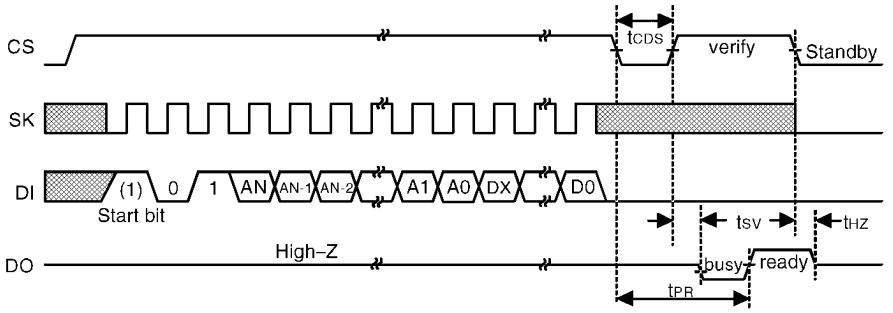
EWEN/EWDS



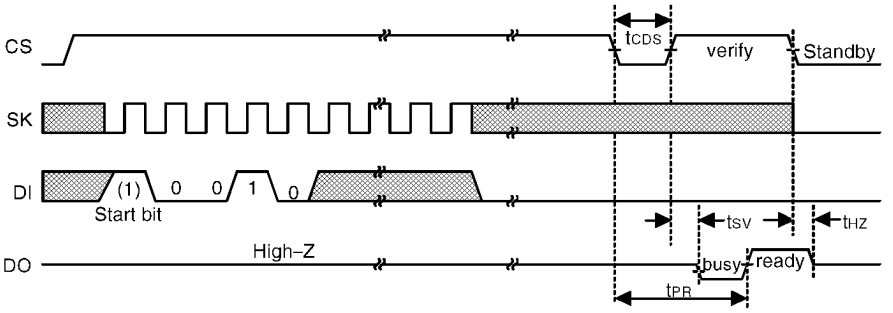
ERASE



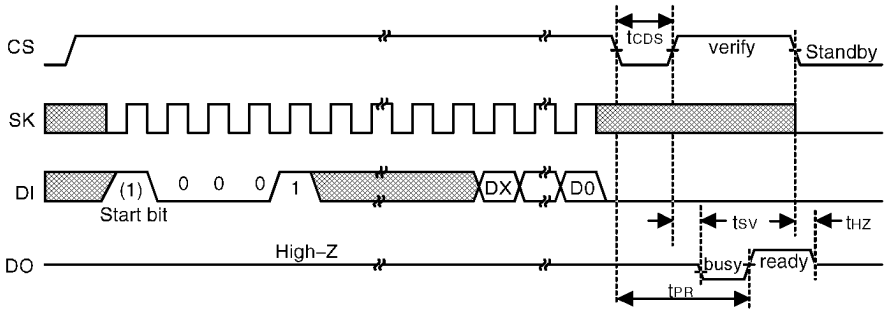
WRITE



ERAL



WRAL



Characteristic Curves